CLAIMS

What is claimed is:

1. An integrated circuit package, comprising:

a first chip having a first side and a second side, the first and second sides having a first plurality of conductive pads formed thereon, at least one conductive pad on the first side being electrically connected to a conductive pad on the second side, the first side containing active circuitry of the first chip;

a first layer formed on the second side and having a first cutout;

a second chip disposed in the first cutout;

a second layer formed on the first layer and having a second cutout;

a third chip disposed in the second cutout;

a third layer formed on the second layer and the third chip; and

an interconnect formed in the one or more of the first, second or third layers to electrically connect at least one conductive pad of the first plurality of conductive pads to one or more of the second and third chips.

2. The integrated circuit package of claim 1, wherein the interconnect further comprises a second plurality of conductive pads on an exposed surface of one or more of the first, second or third layers.

3. The integrated circuit package of claim 1, further comprising:

a polymer layer formed on the first side; and

a second interconnect disposed in the polymer layer, the second interconnect electrically connected to conductive pads of the first plurality of conductive pads on the first side, the second interconnect including third conductive pads on an exposed surface of the polymer layer.

4. The integrated circuit package of claim 1, wherein the first, second and third layers comprise a polymer material.

5. The integrated circuit package of claim 1, further comprising:

a first plurality of conductive bumps electrically connected to conductive pads on the first side of the first chip; and

a second plurality of conductive bumps on at least one exposed surface of one or more of the first, second or third layers, the first chip being disposed between the first and second plurality of conductive bumps.

6. The integrated circuit package of claim 5, further comprising a ball grid array structure coupled to the first plurality of conductive bumps.

7. The integrated circuit package of claim 5, wherein the second plurality of conductive bumps to provide test access points.

8. The integrated circuit package of claim 1, wherein the second chip is joined to the first chip to form a flip-chip structure.

9. The integrated circuit package of claim 1, wherein the interconnect comprises metal deposited in a electroless deposition process.

10. The integrated circuit package of claim 1, wherein the first, second and third chips are thinned chips.

11. The integrated circuit package of claim 1, wherein the first, second and third chips are part of a single wafer before being singulated together in a single package.

12. The integrated circuit package of claim 1, wherein the second chip has a thickness of about 75 μm.

13. The integrated circuit package of claim 1, wherein the third chip has a thickness of about 50 μm.

14. An integrated circuit package, comprising:

a first chip having a first side and a second side, the first and second sides having a first plurality of conductive pads formed thereon, at least one conductive pad on the first side being electrically connected to a conductive pad on the second side, the first side containing active circuitry of the first chip;

a first layer formed on the second side and having a first hole;

a second chip disposed in the first hole;

a second layer formed on the first layer and having a second hole;

a third chip disposed in the second hole;

a third layer formed on the second layer and the third chip; and

an interconnect formed in the one or more of the first, second or third layers to electrically connect at least one conductive pad of the first plurality of conductive pads to one or more of the second and third chips.

15. The integrated circuit package of claim 14, wherein the interconnect further comprises a second plurality of conductive pads on an exposed surface of one or more of the first, second or third layers.

16. The integrated circuit package of claim 14, further comprising:

a polymer layer formed on the first side; and

a second interconnect disposed in the polymer layer, the second interconnect electrically connected to conductive pads of the first plurality of conductive pads on the first side, the second interconnect including third conductive pads on an exposed surface of the polymer layer.

17. The integrated circuit package of claim 14, further comprising:

a first plurality of conductive bumps electrically connected to conductive pads on the first side of the first chip; and

a second plurality of conductive bumps on at least one exposed surface of one or more of the first, second or third layers, the first chip being disposed between the first and second plurality of conductive bumps.

18. An integrated circuit package, comprising:

a first chip having a first side and a second side, the first and second sides having a first plurality of conductive pads formed thereon, at least one conductive pad on the first side being electrically connected to a conductive pad on the second side, the first side containing active circuitry of the first chip;

a first layer formed on the second side and having a first hole;

a second chip disposed in the first hole, wherein the second chip is in contact with the second side;

a second layer formed on the second chip and having a second hole;

a third chip disposed in the second hole, wherein the third chip is in contact with the second chip;

a third layer formed on the third chip; and

an interconnect formed in the one or more of the first, second or third layers to electrically connect at least one conductive pad of the first plurality of conductive pads to one or more of the second and third chips.

19. The integrated circuit package of claim 18, wherein the interconnect further comprises a second plurality of conductive pads on an exposed surface of one or more of the first, second or third layers.

20. The integrated circuit package of claim 18, further comprising:

a polymer layer formed on the first side; and

a second interconnect disposed in the polymer layer, the second interconnect electrically connected to conductive pads of the first plurality of conductive pads on the first side, the second interconnect including third conductive pads on an exposed surface of the polymer layer.